

**Amendments to the Claims**

Claims 1-44 (Cancelled).

45. (Currently amended) A method of forming a semiconductor construction, comprising:

forming a layer of patternable material over a semiconductive substrate material;

patterning the layer of patternable material to form at least two patterned blocks, a pair of adjacent blocks being separated by a first gap;

forming a coating over the pair of adjacent blocks and across the first gap between the adjacent blocks;

selectively removing the coating from across the first gap while leaving the coating along sidewalls and on an upper surface of each of ~~elevationally over~~ the pair of adjacent blocks; the pair of blocks and coating together defining a pair of enlarged blocks that are separated by a second gap; the second gap being narrower than the first gap;

while the enlarged blocks remain over the semiconductive substrate material, implanting at least one dopant within the semiconductive substrate material within the second gap to form a doped region and

removing the enlarged blocks from over the semiconductive substrate material.

46. (Original) The method of claim 45 wherein the patternable material comprises photoresist and wherein the coating comprises a material which cross-links when exposed to the acid from the photoresist.

47. (Original) The method of claim 45 wherein the coating corresponds to a material designated as AZ R200™ by Clariant International, Ltd.

48. (Original) The method of claim 45 wherein the patterned blocks are formed by a photolithographic process; wherein the photolithographic process is limited to a minimum feature size that can be obtained by the photolithographic process, the first gap corresponding to about the minimum feature size; and wherein the doped region of the semiconductive material formed by the implanting has a region width that is less than the minimum feature size.

49. (Original) The method of claim 48 wherein the region width is less than or equal to about 50% of the minimum feature size.

50. (Original) The method of claim 45 further comprising:  
forming a first source/drain region and a second source/drain region within the semiconductive substrate material, the first source/drain region being laterally spaced from a first edge of the doped region and the second source/drain region being laterally spaced from a second opposing edge of the doped region; and

forming an isolation mass over the doped region, the first and second source/drain regions extending partially under the isolation mass.

51. (Original) The method of claim 50 wherein the isolation mass comprises a gate stack, the gate stack comprising a layer of conductively doped material separated from the doped region by an insulative material layer, the layer of conductively doped material being majority doped with a p-type dopant, and wherein the source/drain regions are majority doped with an n-type dopant.

52. (Original) The method of claim 50 further comprising forming a pair of transistor devices over the semiconductor substrate, the transistor devices being electrically isolated from one another by the isolation mass.

Claims 53-64 (Cancelled).

65. (New) The method of claim 45 wherein the removing the enlarged blocks exposes the semiconductive substrate material.

66. (New) The method of claim 45 wherein the removing the enlarged blocks exposes an oxide layer disposed over the semiconductive substrate material.